

07/25/00  
jc893 U.S. PTO

07-26-00

A

**WILLIAMS, MORGAN & AMERSON, P.C.**

7676 HILLMONT, SUITE 250, HOUSTON, TX 77040  
(713) 934-7000 FAX (713) 934-7011

Danny L. Williams  
Terry D. Morgan  
J. Mike Amerson  
Kenneth D. Goodman  
Barbara S. Kitchell, Ph.D.  
Jeffrey A. Pyle  
Randall C. Furlong, Ph.D.

Scott F. Diring\*  
George J. Oehling\*  
Shelley P.M. Fussey, Ph.D.\*  
Mark D. Moore, Ph.D.\*  
Carolanne M. King\*  
Louis H. Iselin, Ph.D.\*  
Raymund F. Eich, Ph.D.\*

jc893 U.S. PTO  
09/29/00  
07/25/00

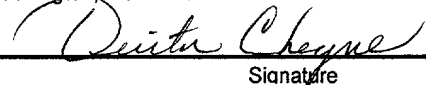
\*Patent Agent

Writer's Direct Dial  
(713) 934-4055

File: 2000.043500

July 25, 2000

**BOX PATENT APPLICATION**  
Assistant Commissioner for Patents  
Washington, DC 20231

<b>EXPRESS MAIL RECEIPT</b>	
NUMBER:	EL522495267US
DATE OF DEPOSIT:	JULY 25, 2000
I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, DC 20231.	
	
Signature	

RE: *U.S. Patent Application Entitled: METHOD OF CONTROLLING SHEET RESISTANCE OF METAL SILICIDE REGIONS BY CONTROLLING THE SALICIDE STRIP TIME – H. Jim Fulford (2000.043500/TT3203)*

Sir:

Transmitted herewith for filing are:

- (1) 22-page patent specification with 27 claims and an abstract (also Figures 1-6 on 4 sheets);
- (2) Declaration;
- (3) Power of Attorney; and
- (4) Assignment and Assignment Cover Sheet.

All correspondence, notices, official letters and other communications should be directed to J. Mike Amerson, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, TX 77040, and all telephone calls should be directed to J. Mike Amerson at (713) 934-4055.

The Assistant Commissioner is authorized to deduct the amount of the total filing fee (listed below) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT3203.

0962495267US

Assistant Commissioner for Patents

July 25, 2000

Page 2

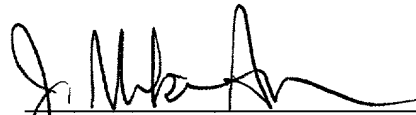
**FILING FEE CALCULATION**

FOR		Small Entity	Large Entity
Total Claims	27 - 20 = 7	x \$9 = \$	or x \$18 = \$ 126.00
Independent Claims	3 - 3 = 0	x \$39 = \$	or x \$78 = \$ 0.00
Multiple Dependent Claim(s)		+ \$130 = \$	or + \$260 = \$ 0.00
Basic Fee:		+ \$345 = \$	or + \$690 = \$ 690.00
Assignment Recording Fee:	(\$40 per assignee)	+ = \$	+ = \$ 40.00
<b>TOTAL FILING FEES</b>		<b>\$ <u>0.00</u></b>	<b>\$ <u>856.00</u></b>

Pursuant to 37 C.F.R. § 1.10 the Applicants request the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail.

Please date stamp and return the enclosed postcards to evidence receipt of these materials.

Respectfully submitted,



J. Mike Amerson

Reg. No. 35,426

WILLIAMS, MORGAN & AMERSON, P.C.

7676 Hillmont, Suite 250

Houston, TX 77040

(713) 934-4055

Attorneys for Applicants

JMA/mp

Enclosures

cc: Ms. Samantha Cardona (w/enc.)

005229 254260

Application for United States Letters Patent

for

**METHOD OF CONTROLLING SHEET RESISTANCE OF METAL  
SILICIDE REGIONS BY CONTROLLING THE SALICIDE STRIP  
TIME**

by

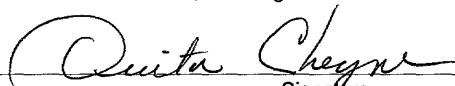
**H. Jim Fulford**

EXPRESS MAIL MAILING LABEL

NUMBER EL522495267US

DATE OF DEPOSIT July 25, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington D.C. 20231.

  
Signature

# METHOD OF CONTROLLING SHEET RESISTANCE OF METAL SILICIDE REGIONS BY CONTROLLING THE SALICIDE STRIP TIME

## BACKGROUND OF THE INVENTION

### 1. FIELD OF THE INVENTION

This invention relates generally to semiconductor device manufacturing, and, more particularly, to a method of controlling sheet resistance of metal silicide regions by controlling the salicide strip time.

### 2. DESCRIPTION OF THE RELATED ART

The manufacture of most devices, such as semiconductor devices, requires a number of discrete processing steps to create the device. With respect to semiconductor devices, a number of discrete steps are needed to produce a packaged semiconductor circuit device from raw semiconductor material. The starting substrate is usually a slice of single crystal silicon referred to as a wafer. Circuits of a particular type are fabricated together in batches of wafers called "lots" or "runs." The fabrication process creates regular arrays of a circuit on the wafers of a lot. During processing, the individual wafers in a lot may go through individual processing steps one at a time or as a batch. At the completion of wafer processing, the wafers are tested to determine circuit functionality. Later, the wafers are cut to separate the individual integrated circuit devices, the functioning devices are packaged, and further testing is performed prior to use by the customer.

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, *e.g.*, microprocessors, memory devices, etc. This drive is fueled by consumer demands for computers and electronic devices that operate at increas-

ingly greater speeds. By way of background, Figure 1 depicts an illustrative NMOS field effect transistor 10 formed above a surface 14 of a semiconducting substrate 12 between trench isolation regions 25. The transistor 10 is comprised of a gate dielectric 16, a gate electrode 18, a plurality of sidewall spacers 20 and multiple source/drain regions 28. The transistor 10 is further comprised of metal silicide regions 21 formed on the source/drain regions 28 and on the gate electrode 18.

The purpose of the metal silicide regions 21 is to reduce the contact resistance of the source/drain regions 28 and the gate electrode 18. The metal silicide regions 21 are formed by depositing a layer of refractory metal, *e.g.*, cobalt, titanium, etc., above the source/drain regions 28 and the gate electrode 18. Thereafter, by performing one or more anneal processes, portions of the refractory metal layer in contact with the source/drain regions 28 and the gate electrode 18 are converted to a metal silicide, *e.g.*, cobalt silicide, titanium silicide, etc.

In the process of forming the metal silicide regions 21 above the source/drain regions 28 and above the gate electrode 18, there comes a point where unreacted portions of the initially-formed layer of refractory metal are removed. For example, in areas where the refractory metal layer is not in contact with polysilicon, *e.g.*, the surface of the sidewall spacers 20, the refractory metal layer will not be converted to a metal silicide. This removal of the unreacted refractory metal layer is typically accomplished by a dilute acid bath, such as a bath comprised of sulfuric acid and hydrogen peroxide. During this process, portions of the previously formed metal silicide contacts 21 are removed. This, in turn, increases the sheet resistance of the contact, thereby making the operation of the device slower and less efficient, both of which are undesirable.

However, due to the construction of the device, it is imperative that no “bridging” material is left between the metal silicide regions formed above the source/drain regions 28 and the gate electrode 18. Otherwise, a short circuit path may be established that may severely hamper or prevent the functioning of this device. Thus, in an effort to insure that essentially all of the unreacted refractory metal is removed from places where it should not be, the removal process is designed for a “worst-case” situation. That is, the parameters of the removal process used to remove the unreacted refractory metal are set based upon the greatest thickness anticipated for the refractory metal, *i.e.*, existing methods set the duration of the chemical removal process based upon the thickest layer of refractory metal that may be anticipated by the process. In situations where the layer of refractory metal is less than the maximum thickness anticipated by the design process, this results in subjecting the device to the etching process for a duration longer than would otherwise be required to remove the unreacted portions of the layer of refractory metal. In turn, this over-etching needlessly consumes some of the thickness of the metal silicide regions 21, which undesirably increases the sheet resistance of the metal silicide regions 21.

The present invention is directed to a method of forming a semiconductor device that minimizes or reduces some or all of the aforementioned problems.

### **SUMMARY OF THE INVENTION**

The present invention is directed to a method of controlling the sheet resistance of metal silicide regions by controlling the silicide strip time. In one illustrative embodiment, the method comprises forming a layer comprised of a refractory metal, determining a thickness of the layer of refractory metal, and converting a portion of the layer of refractory metal

to a metal silicide. The method further comprises determining a duration of an etching process to be used to remove unreacted portions of the refractory metal layer based upon the determined thickness of the refractory metal layer, and performing the etching process for the determined duration.

5

### **BRIEF DESCRIPTION OF THE DRAWINGS**

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view of an illustrative prior art transistor;

Figure 2 is a cross-sectional view of a partially formed transistor;

Figure 3 is a cross-sectional view of the device shown in Figure 2 after a layer of refractory metal has been formed thereabove;

Figure 4 is a cross-sectional view of the device shown in Figure 3 after portions of the layer of refractory metal have been converted to a metal silicide;

Figure 5 is a depiction of an illustrative system that may be used with the present invention; and

Figure 6 is a flowchart depicting one illustrative embodiment of the inventive methods disclosed herein.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

### **DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS**

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to Figures 2-6. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features depicted in the drawings may be exaggerated or reduced as compared to the size of those feature sizes on fabricated devices. Never-



theless, the attached drawings are included to describe and explain illustrative examples of the present invention.

In general, the present invention is directed to a method of controlling the sheet resistance of metal silicide regions by controlling the silicide strip time. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, *e.g.*, NMOS, PMOS, CMOS, etc., is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc.

As shown in Figure 2, an illustrative NMOS field effect transistor 30 is formed above a surface 34 of a semiconducting substrate 32. Although the transistor 30 depicted in Figure 2 is an NMOS transistor, the present invention is not limited to any particular technology. At this stage of fabrication, the transistor 30 is comprised of a gate insulation layer 36, a gate electrode 38, and sidewall spacers 43. In general, the particular materials and techniques used to form the various components and layers depicted in Figure 2, *e.g.*, the gate insulation layer 36 and the gate electrode 38, are matters of design choice, and, thus, should not be considered a limitation of the present invention. For example, the gate insulation layer 36 may be comprised of silicon dioxide, and it may be formed by thermal growth or deposition process. Similarly, the gate electrode layer 38 may be comprised of polysilicon, and it may be formed by a physical vapor deposition ("PVD") or a chemical vapor deposition ("CVD") process. In one illustrative embodiment, the gate electrode 38 is comprised of a layer of polysilicon having a thickness ranging from approximately 2000-4000 Å that is formed by a CVD process. The structure comprised of the gate insulation layer 36 and the gate electrode

38 may be formed by forming the various process layers for those components and thereafter patterning these layers using known photolithography and etching techniques.

The sidewall spacers 43 are formed adjacent the gate electrode 38 and the gate insulation layer 36. The sidewall spacers 43 may be formed by blanket-depositing a layer of spacer material (not shown) over the transistor 30, and thereafter performing an anisotropic etching process. As will be apparent to those skilled in the art upon a complete reading of the present application, the sidewall spacers 43 may be formed from any of a variety of materials, such as silicon dioxide, silicon nitride, etc. Moreover, although single sidewall spacers 43 are depicted in Figure 2, the present invention may be used in situations where multiple sidewall spacers are formed adjacent each side 33 of the gate electrode 38.

Source/drain regions 47 are also formed in the substrate 32 by implanting dopant atoms, *e.g.*, arsenic, boron, etc., into the substrate using one or more ion implantation processes. For example, prior to the formation of the sidewall spacer 43, the transistor 30 may be subjected to an ion implantation process with the appropriate dopant atoms at a relatively light doping concentration to form a relatively shallow dopant implant region (not shown) that is self-aligned with respect to the gate electrode 38. After formation of the sidewall spacers 43, the transistor 30 is then subjected to another ion implantation process to complete the formation of the source/drain regions 47 depicted in Figure 2. The described process flow results in source/drain regions 47 having the familiar lightly-doped ("LDD") structure. Of course, the formation of source/drain regions 47 using the particular methods or processes described herein is not required to practice the present invention.

Next, as shown in Figure 3, a layer of refractory metal 40 may be formed above the gate electrode 38, the sidewall spacers 43, and a surface 53 of the source/drain regions 47. The layer of refractory metal 40 may be comprised of any metal that may subsequently be converted into a metal silicide. For example, the layer of refractory metal 40 may be comprised of cobalt, titanium, tantalum, platinum, nickel, or other like materials. The layer of refractory metal 40 may have a thickness ranging from approximately 50-200 Å, and it may be formed by any of a variety of known techniques for forming such layers, *e.g.*, PVD, CVD, etc. In one illustrative embodiment, the layer of refractory metal 40 is comprised of cobalt having a thickness ranging from approximately 50-200 Å that is formed by a PVD process.

Thereafter, at least portions of the layer of refractory metal 40 are converted to metal silicide regions 57 by performing one or more anneal processes. In particular, during the anneal process, portions of the layer of refractory metal 40 in contact with the surface 53 of the source/drain regions 47 and a surface 27 of the gate electrode 38 are converted to metal silicide regions 57. Portions of the refractory metal layer 40 that are unreacted after this conversion process may be removed by a subsequent acid rinse, for example, H<sub>2</sub>O<sub>2</sub> plus water, to result in the structure depicted in Figure 4.

The particular parameters of the anneal process or processes used to form the metal silicide regions 57 are matters of design choice, and they may vary depending upon the device under construction as well as the thickness and composition of the layer of refractory metal 40. The anneal process may be comprised of a one-step or a two-step anneal process in a rapid thermal anneal chamber. The duration and temperatures of the anneal process may be varied as a matter of design choice to insure that the layer of refractory metal 40 reaches the

appropriate temperature. In one illustrative example, where the layer of refractory metal 40 is comprised of approximately 50-200 Å of cobalt, the anneal process may be comprised of a first step at about 450-600°C for a duration of approximately 10-90 seconds, and a second step at about 650-900°C for a duration of approximately 10-90 seconds.

5

In one embodiment of the present invention, the process of removing the unreacted portions of the refractory metal layer 40 is adjusted, depending upon the thickness of the refractory metal layer 40. One illustrative system that may be used in accordance with the present invention is depicted in Figure 5. As shown therein, a system 60 for processing wafers 61 is comprised of a process tool 62 used for forming the refractory metal layer 40, *e.g.*, a deposition tool, a metrology tool 64, an automatic process controller 66, and an etch tool 68. The metrology tool 64 is used to measure the as-formed thickness of the refractory metal layer 40.

10

15

In one embodiment, the automatic process controller 66 interfaces with the metrology tool 64 and the etch tool 68 to control the duration of the processing performed in the etch tool 68, depending upon the thickness of the refractory metal layer 40, as determined by the metrology tool 64. That is, the thickness of the refractory metal layer 40 is fed forward to the controller 66, and the resident time in the etch tool 68 is controlled based upon this measured thickness. For example, the greater the thickness of the refractory metal layer 40, the longer the resident time in the etch tool 68. Conversely, the thinner the refractory metal layer 40, the shorter the resident time in the etch tool 68.

20

25

The metrology tool 64 may be any type of device capable of measuring the thickness of such process layers, *e.g.*, an acoustic wave metrology tool, such as the Metapulse tool

manufactured by Rudolph. Another technique for measuring this thickness is known as Ruckerford back scattering (RBS). Moreover, the metrology tool 64 may be a stand-alone device or system, or it may be incorporated into the process tool 62, or a system containing both. The etch tool 68 is used to remove the unreacted portions of the refractory metal layer 40 after silicidation processing has been performed to form the various metal silicide regions 57 described above. The etch tool 68 may be comprised of a variety of wet etching systems useful for removing the unreacted portions of the refractory metal layer 40. Moreover, the particular etch chemistry used in the etch tool 68 may vary depending upon the device under construction as well as the material comprising the refractory metal layer 40.

In the illustrated embodiment, the automatic process controller 66 is a computer programmed with software to implement the functions described. However, as will be appreciated by those of ordinary skill in the art, a hardware controller (not shown) designed to implement the particular functions may also be used. Portions of the invention and corresponding detailed description are presented in terms of software, or algorithms and symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the ones by which those of ordinary skill in the art effectively convey the substance of their work to others of ordinary skill in the art. An algorithm, as the term is used here, and as it is used generally, is conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of optical, electrical, or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise, or as is apparent from the discussion, terms such as “processing” or “computing” or “calculating” or “determining” or “displaying” or the like, refer to the actions and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical, electronic quantities within the computer system’s registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

An exemplary software system capable of being adapted to perform the functions of the automatic process controller 66, as described, is the Catalyst system offered by KLA Tencor. The Catalyst system uses Semiconductor Equipment and Materials International (SEMI) Computer Integrated Manufacturing (CIM) Framework compliant system technologies, and is based on the Advanced Process Control (APC) Framework. CIM (SEMI E81-0699 - Provisional Specification for CIM Framework Domain Architecture) and APC (SEMI E93-0999 - Provisional Specification for CIM Framework Advanced Process Control Component) specifications are publicly available from SEMI.

Referring now to Figure 6, a flow diagram of a method for controlling the sheet resistance of metal silicide regions by controlling silicide strip time is provided. As depicted therein, the method comprises forming a layer comprised of a refractory metal, as indicated at block 70, and determining a thickness of the layer of refractory metal, as indicated at block 72. The method further comprises converting a portion of the refractory metal layer to a

metal silicide, as indicated at block 74, determining the duration of a wet etching process to be used to remove unreacted portions of the layer of refractory metal based upon the determined thickness of the refractory metal layer, as indicated at block 76, and performing the etching process for the determined duration, as indicated at block 78.

5

As described above, the step of forming the layer of refractory metal, as recited at block 70, may be performed by any process tool useful for such purposes, *e.g.*, a chemical vapor deposition ("CVD") tool, a physical vapor deposition ("PVD") tool, a plasma enhanced chemical vapor deposition ("PECVD") tool, etc. Moreover, the refractory metal layer formed during this step may be comprised of a variety of materials, *e.g.*, cobalt, titanium, etc. The thickness of the layer of refractory metal may also be varied as a matter of design choice.

Similarly, the thickness of the refractory metal layer 40 may be determined using any tool suitable for such purposes. Moreover, this thickness determination may be based on a single or multiple measurements, it may represent a mean or median of a group of measurements, or it may otherwise reflect statistical sampling of a sufficient quantity and at sufficient locations to provide a degree of reliability as to its accuracy that is sufficient for use in the present invention.

The step of converting a portion of the refractory metal layer to a metal silicide, as set forth at block 74, may be accomplished by performing one or more anneal steps in the appropriate process tool, *e.g.*, a rapid thermal anneal chamber. The exact parameters of the anneal process or processes may vary depending upon the device under construction and the materials comprising the refractory metal layer 40. Thus, the illustrative anneal processes described herein should not be considered a limitation of the present invention.

As set forth in block 76, the step of determining the duration of the etching process to remove the unreacted portions of the refractory metal layer based upon the determined thickness of the refractory metal layer may be performed by a variety of techniques. For example, a database may be developed that correlates the determined thickness of the refractory metal layer to a corresponding etch duration, depending upon the composition and concentrations of the components of the etch bath. Alternatively, the etch duration could be calculated based upon a known etch rate of the material comprising the refractory metal layer and its thickness. Other methodologies are also possible. Thereafter, as indicated at block 78, the method continues with performing the etch process for the determined time period to remove the unreacted portion of the refractory metal layer 40.

Through use of the present invention, the sheet resistance of the metal silicide regions on a semiconductor device may be controlled by controlling the silicide strip time. The present invention may be used to reduce or eliminate excessive consumption of metal silicide regions during silicide stripping operations. This will, in turn, help prevent the increase in the sheet resistance of the regions, thereby helping to insure device integrity and performance.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered



or modified and all such variations are considered within the scope and spirit of the invention.

Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A method comprising:

forming a layer comprised of a refractory metal;

determining a thickness of said layer of refractory metal;

converting a portion of said layer of refractory metal to a metal silicide;

determining a duration of an etching process to remove unreacted portions of said

refractory metal layer based upon said determined thickness of said refractory

metal layer; and

performing said etching process for said determined duration to remove said

unreacted portions of said refractory metal layer.

2. The method of claim 1, wherein forming a layer comprised of a refractory metal comprises depositing a layer comprised of a refractory metal.

3. The method of claim 1, wherein forming a layer comprised of a refractory metal comprises forming a layer comprised of a refractory metal comprised of at least one of cobalt, titanium, tantalum and nickel.

4. The method of claim 1, wherein forming a layer comprised of a refractory metal comprises forming a layer comprised of a refractory metal above a plurality of source/drain regions and a gate electrode of a transistor.

5. The method of claim 1, wherein determining a thickness of said layer of refractory metal comprises determining a thickness of said layer of refractory metal based upon a single measurement of said layer of refractory metal.

5 6. The method of claim 1, wherein determining a thickness of said layer of refractory metal comprises determining a thickness of said layer of refractory metal based upon multiple measurements of said layer of refractory metal.

10 7. The method of claim 1, wherein determining a thickness of said layer of refractory metal comprises determining an average thickness of said layer of refractory metal.

15 8. The method of claim 1, wherein converting a portion of said layer of refractory metal to a metal silicide comprises performing at least one anneal process to convert a portion of said layer of refractory metal to a metal silicide.

9. The method of claim 1, wherein converting a portion of said layer of refractory metal to a metal silicide comprises performing at least two anneal processes to convert a portion of said layer of refractory metal to a metal silicide.

20 10. The method of claim 1, wherein determining a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer comprises calculating a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer.

11. The method of claim 1, wherein determining a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer comprises selecting a duration of an etching process to remove unreacted portions of said refractory metal layer from a database that correlates the duration of the etching process to said determined thickness of said refractory metal layer.

12. A method comprising:

depositing a layer comprised of a refractory metal above a plurality of source/drain regions and a gate electrode of a transistor;

determining a thickness of said layer of refractory metal;

converting a portion of said layer of refractory metal to a metal silicide by performing at least one anneal process;

determining a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer; and

performing said etching process for said determined duration to remove said unreacted portions of said refractory metal layer.

13. The method of claim 12, wherein depositing a layer comprised of a refractory metal comprises depositing a layer comprised of a refractory metal comprised of at least one of cobalt, titanium, tantalum and nickel.

14. The method of claim 12, wherein determining a thickness of said layer of refractory metal comprises determining a thickness of said layer of refractory metal based upon a single measurement of said layer of refractory metal.

15. The method of claim 12, wherein determining a thickness of said layer of refractory metal comprises determining a thickness of said layer of refractory metal based upon multiple measurements of said layer of refractory metal.

5

16. The method of claim 12, wherein determining a thickness of said layer of refractory metal comprises determining an average thickness of said layer of refractory metal.

17. The method of claim 12, wherein converting a portion of said layer of refractory metal to a metal silicide by performing at least one anneal process comprises converting a portion of said layer of refractory metal to a metal silicide by performing at least two anneal processes.

18. The method of claim 12, wherein determining a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer comprises calculating a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer.

19. The method of claim 12, wherein determining a duration of an etching process to remove unreacted portions of said refractory metal layer based upon said determined thickness of said refractory metal layer comprises selecting a duration of an etching process to remove unreacted portions of said refractory metal layer from a database that correlates the duration of the etching process to said determined thickness of said refractory metal layer.

25

20. A system, comprising:

a process tool for forming a layer of refractory metal above a plurality of source/drain regions and a gate electrode of a transistor;

a metrology tool, said metrology tool adapted for determining a thickness of said layer of refractory metal;

an etching tool for performing an etching process to remove unreacted portions of said refractory metal layer after portions of the refractory metal layer have been converted to a metal silicide; and

a controller that determines a duration of said etching process based upon said thickness determined by said metrology tool.

21. The system of claim 20, wherein said process tool is a deposition tool.

22. The system of claim 20, wherein said metrology tool is an acoustic wave metrology tool.

23. The system of claim 20, wherein said metrology tool determines an average thickness of said layer of refractory metal.

24. The system of claim 20, wherein said metrology tool determines a thickness based upon a single measurement of said refractory metal layer.

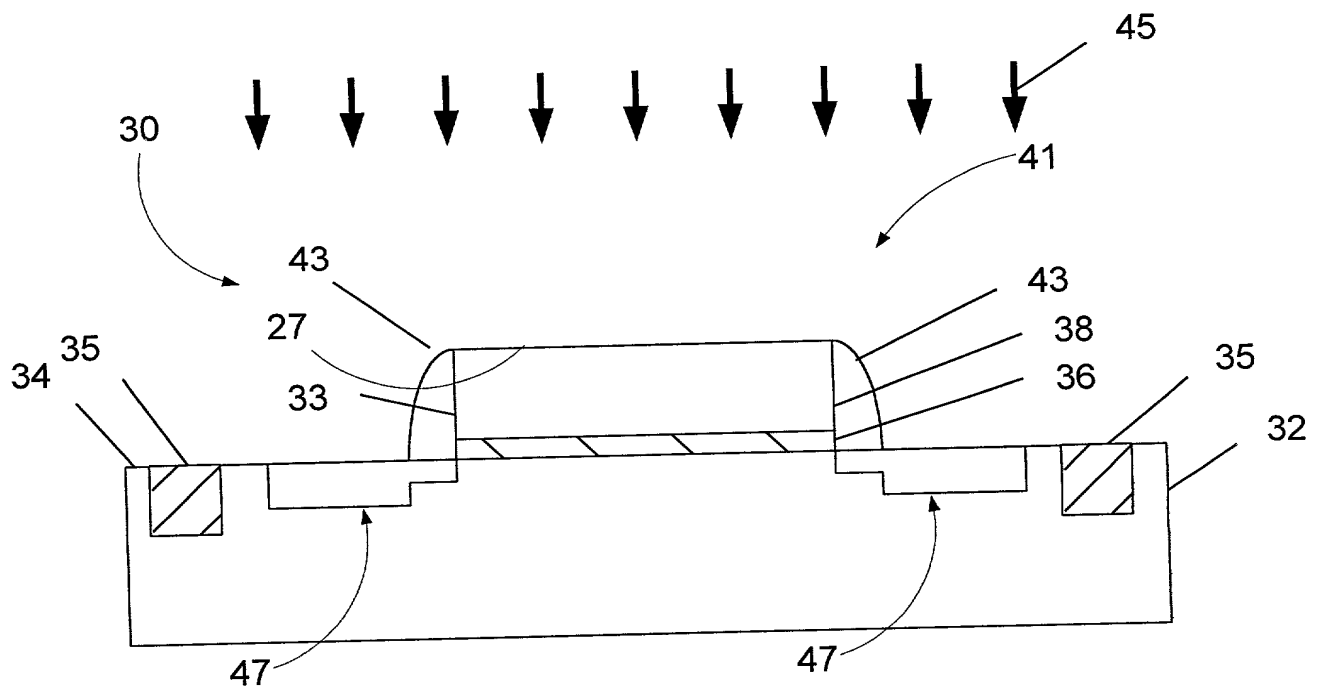
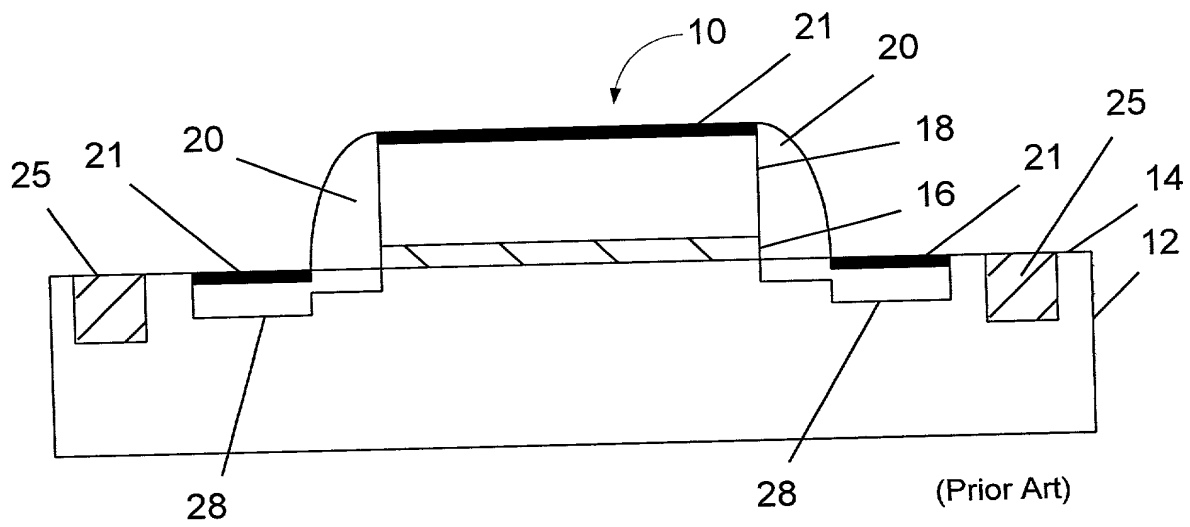
25. The system of claim 20, wherein said metrology tool determines a thickness based upon multiple measurements of said refractory metal layer.

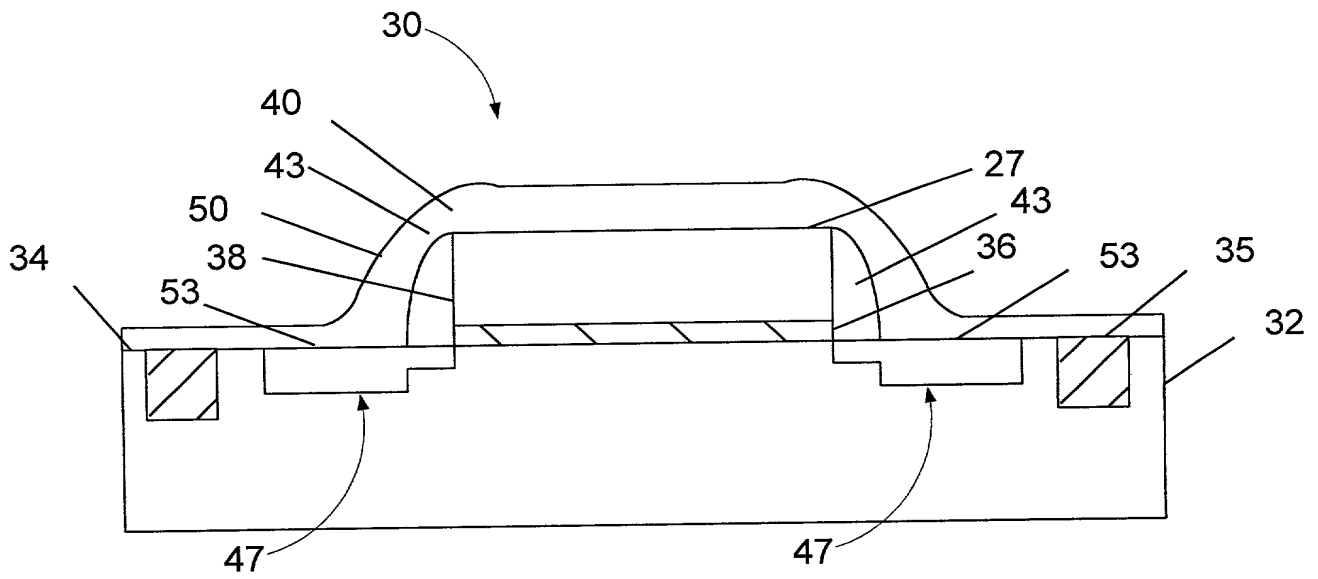
26. The system of claim 20, wherein said controller is a stand-alone controller.
27. The system of claim 20, wherein said controller is coupled to said etching tool.

**ABSTRACT OF THE DISCLOSURE**

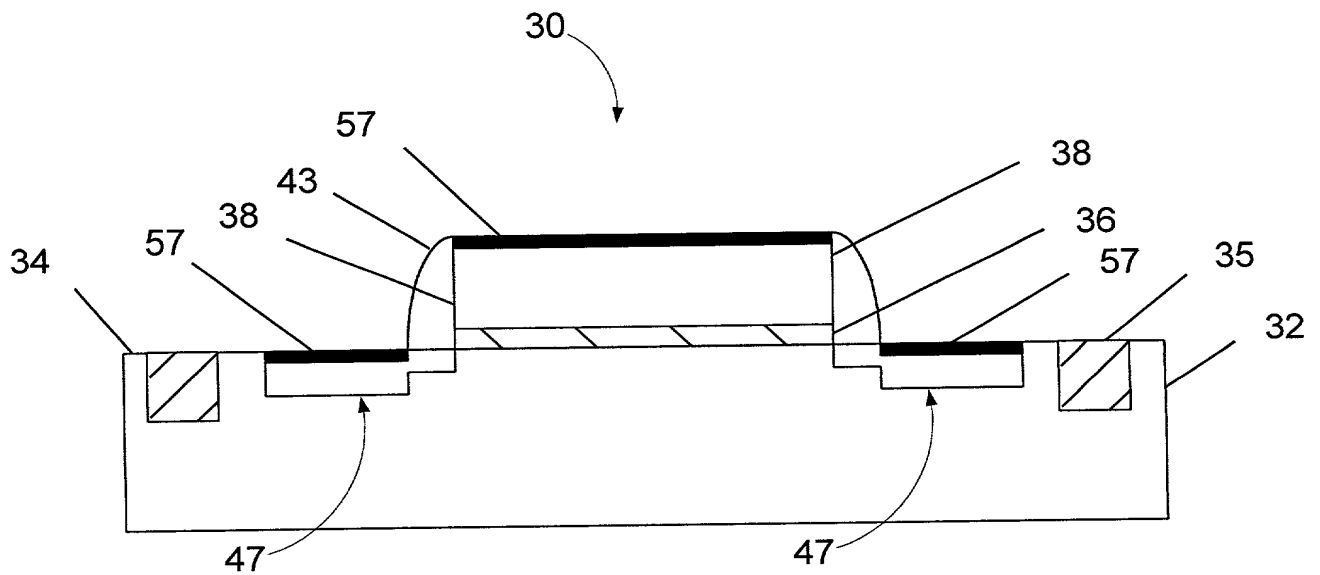
A method of controlling the sheet resistance of metal silicide regions by controlling the silicide strip time is provided. In one illustrative embodiment, the method comprises forming a layer comprised of a refractory metal, determining a thickness of the layer of refractory metal, and converting a portion of the layer of refractory metal to a metal silicide. The method further comprises determining a duration of an etching process to be used to remove unreacted portions of the refractory metal layer based upon the determined thickness of the refractory metal layer, and performing the etching process for the determined duration.





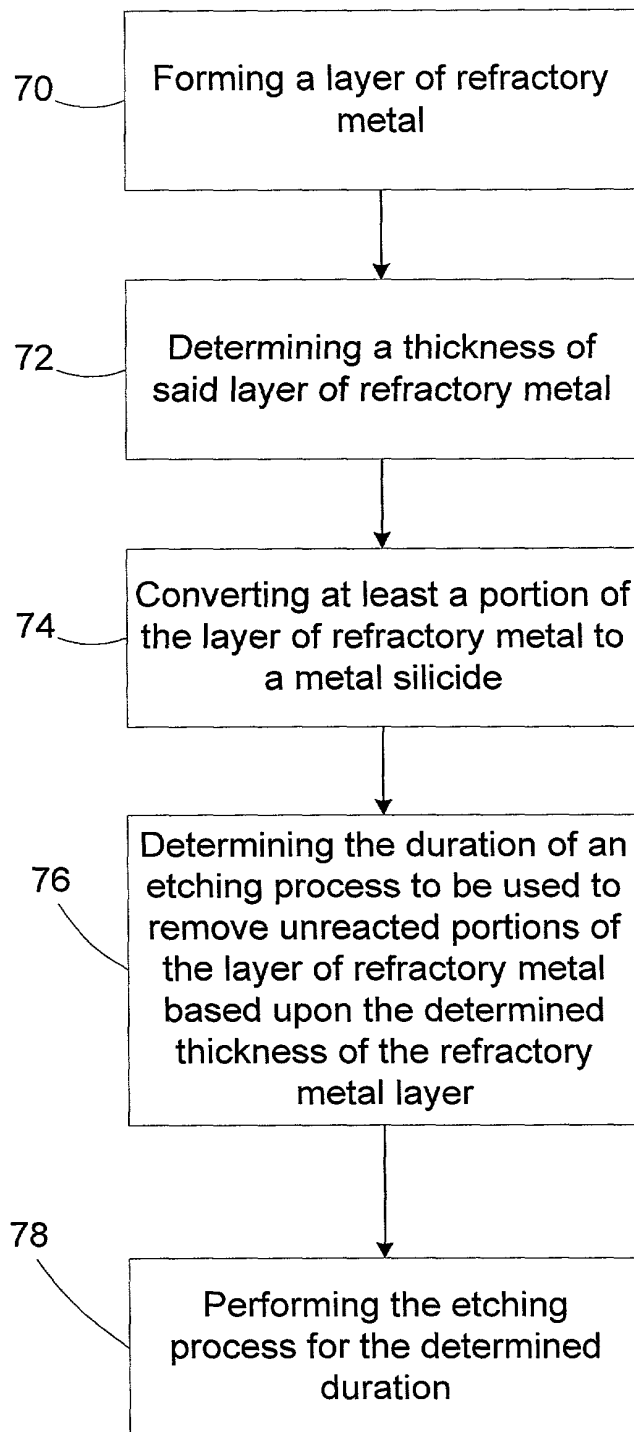


**FIG. 3**



**FIG. 4**

### Fig. 5



**Fig. 6**

**DECLARATION**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "**METHOD OF CONTROLLING SHEET RESISTANCE OF METAL SILICIDE REGIONS BY CONTROLLING THE SALICIDE STRIP TIME**" the Specification of which:

☒ is attached hereto.  
☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent, United States provisional application(s), or inventor's certificate listed below and have also identified below any foreign application for patent, United States provisional application, or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIORITY APPLICATION(S)			Priority Claimed
(Number)	(Country)	(Date Filed)	Yes/No
(Number)	(Country)	(Date Filed)	Yes/No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

I hereby direct that all correspondence and telephone calls be addressed to J. Mike Amerson, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, Texas 77040, (713) 934-7000.

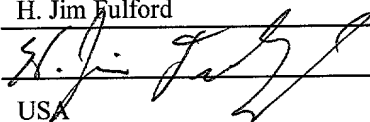
00524656-072500

I HEREBY DECLARE THAT ALL STATEMENTS MADE OF MY OWN KNOWLEDGE ARE TRUE AND THAT ALL STATEMENTS MADE ON INFORMATION AND BELIEF ARE BELIEVED TO BE TRUE; AND FURTHER THAT THESE STATEMENTS WERE MADE WITH THE KNOWLEDGE THAT WILLFUL FALSE STATEMENTS AND THE LIKE SO MADE ARE PUNISHABLE BY FINE OR IMPRISONMENT, OR BOTH, UNDER SECTION 1001 OF TITLE 18 OF THE UNITED STATES CODE AND THAT SUCH WILLFUL FALSE STATEMENTS MAY JEOPARDIZE THE VALIDITY OF THE APPLICATION OR ANY PATENT ISSUED THEREON.

Inventor's Full Name:

H. Jim Fulford

Inventor's Signature:



Country of Citizenship:

USA

Date:

9/13/00

Residence Address: (street,  
number, city, state, and/or  
country)

9808 Woodshire Drive

Austin, TX 78748

Post Office Address:  
(if different from above)

Same

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: §  
H. JIM FULFORD §  
Serial No.: Unknown § Examiner: Unknown  
Filed: Concurrently Herewith § Group Art Unit: Unknown  
FOR: METHOD OF CONTROLLING SHEET § Att'y Docket: 2000.043500/TT3203  
RESISTANCE OF METAL SILICIDE §  
REGIONS BY CONTROLLING THE §  
SALICIDE STRIP TIME §

**POWER OF ATTORNEY**

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

The undersigned, being the inventors named in the above-identified application, hereby revoke any previous Powers of Attorney and appoint:

Elizabeth A. Apperley, Reg. No. 36,428; Paul S. Drake, Reg. No. 33,491; Louis A. Riley, Reg. No. 39,817; Richard J. Roddy, Reg. No. 27,688; William D. Zahrt II, Reg. No. 26,070; and; Harry A. Wolin, Reg. No. 32,638 of Advanced Micro Devices, Inc.; and

Danny L. Williams, Reg. No. 31,892; Terry D. Morgan, Reg. No. 31,181; J. Mike Amerson, Reg. No. 35,426; Kenneth D. Goodman, Reg. No. 30,460; Barbara S. Kitchell, Reg. No. 33,928; Jeffrey A. Pyle, Reg. No. 34,904; Randall C. Furlong, Reg. No. 35,144; Scott F. Diring, Reg. No. 35,119; George J. Oehling, Reg. No. 40,471; Shelley P.M. Fussey, Reg. No. 39,458; Mark D. Moore, Reg. No. 42,903; Carolanne M. King, Reg. No. 44,914; Louis H. Iselin, Reg. No. 42,684; and Raymund F. Eich, Reg. No. 42,508; of Williams, Morgan & Amerson, P.C.,

as its attorney or agent so long as they remain with such firms, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Please direct all communications as follows:

J. Mike Amerson  
WILLIAMS, MORGAN & AMERSON, P.C.  
7676 Hillmont, Suite 250  
Houston, Texas 77040  
(713) 934-7000

Signature:

H. Jim Fulford

Date:

7/13/00

005270 95942960